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APPLICATION FOR PATENT

Buried Heterostructure Device Fabricated by Single Step MOCVD

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Background

[0001] Optoelectronic devices are used in many applications including telecommunications, data storage and signalling. Certain types of optoelectronic devices such as laser diodes, optoelectronic modulators, semiconductor optical amplifiers, semiconductor gain media, etc., have an active region located in an optical waveguide. The optical waveguide typically incorporates different structures to guide the light laterally, i.e., parallel to the major surface of the substrate on which the device is fabricated, and transversely, i.e., orthogonal to the major surface of the substrate. In the transverse direction, the light is guided by a refractive index contrast between the semiconductor material of the active region and cladding layers between which the active layer is sandwiched. In the lateral direction, the light is guided by a ridge waveguide structure or a buried heterostructure waveguide defined at least in part in the layer structure of which the cladding layers and the active region form part.

[0002] In telecommunications applications, the most commonly used lateral waveguide structure is the buried heterostructure. A buried heterostructure provides advantages over a ridge waveguide structure because of the large refractive index contrast it provides at the active region. This allows the optical waveguide to be made very narrow, while preserving a high spatial overlap between the fundamental optical mode and the active region. This provides such advantages as a low threshold current in lasers, a lower operating current in semiconductor optical amplifiers and optical gain media, and a low capacitance, and, hence, increased

modulation speed, in optoelectronic modulators and directly modulated lasers.

[0003] A typical process for fabricating optoelectronic devices incorporating a buried heterostructure lateral waveguide is illustrated in Figures 1A-1C. First, a layer structure 10 from which hundreds or thousands of optoelectronic devices are made is grown. Figures 1A-1C are side views of a portion of layer structure 10 in which a single optoelectronic device is fabricated. Figure 1A shows an n-type cladding layer 12, an undoped active region 14 and a p-type cladding layer 16 grown on a substrate 18. The layers are grown by metal organic chemical vapor deposition (MOCVD), also known in the art as organo-metallic vapor phase epitaxy (OMVPE).

[0004] The materials of layer structure 10 are Group III-V semiconductors typically composed of such elements as indium, gallium, arsenic and phosphorus. The semiconductor material of cladding layers 12 and 16 has a lower refractive index than that of active region 14. The thickness of n-type cladding layer 12 is about 2 μm, whereas the thickness of p-type cladding layer 16 in layer structure 10 is only about 200nm-400nm.

[0005] A quantum well structure 20 composed of one or more quantum wells is located in active region 14. Each quantum well is defined by a quantum well layer of low band-gap semiconductor material sandwiched between barrier layers of higher band-gap semiconductor material.

[0006] Figure 1A also shows a mask 22 deposited on the surface of p-type cladding layer 16. The material of the mask is typically silicon dioxide. Mask 22 is elongate in the *y*-direction shown in Figure 1A, and is typically about 1-8 μm wide.

[0007] Layer structure 10 is then removed from the growth chamber and is subject to two etching processes that define a mesa 24 in the layer structure, as shown in Figure 1B. A reactive ion etch (RIE) is initially used to remove portions of p-type cladding layer 16, active region 14 and n-type cladding layer 12 not protected by mask 22. The RIE damages the edges of the layers subject to etching. Such damaged edges significantly impair the efficiency of the finished optoelectronic device. Accordingly, layer structure 10 is additionally subject to a wet etch that removes the damaged edges of p-type cladding layer 16, active region 14 and n-type cladding layer 12. The wet etch process additionally defines the overhang of mask 22 relative to mesa 24. Figure 1B shows layer structure 10 after both etching processes have

been performed.

[0008] Layer structure 10 is then returned to the growth chamber, and an overgrowth 26 of a high resistivity group III-V semiconductor material having a lower refractive index than the materials of active region 14 is epitaxially grown on the layer structure by MOCVD, as shown in Figure 1C. The overgrowth grows on the exposed surface of substrate 18 and on the sidewalls of mesa 24, but does not grow on mask 22. Accordingly, overgrowth 26 fills the cavities etched into the layer structure between adjacent mesas. Deposition of the overgrowth continues until its growth surface reaches the top surface of p-type cladding layer 16.

[0009] In an embodiment of layer structure 10 in which the material of cladding layers 12 and 16 is indium phosphide (InP), a typical material of overgrowth 26 is indium phosphide doped with iron (InP:Fe). The refractive index of the overgrowth material is about 0.2 less than that of the materials of active region 14. The overgrowth material is doped with iron (Fe) to reduce its conductivity.

[0010] Layer structure 10 is then removed from the growth chamber and is subject to another wet etch process that removes the mask 22 from the surface of p-type cladding layer 16.

[0011] Layer structure 10 is then returned to the growth chamber, where additional p-type cladding layer material 28 is grown over the exposed surfaces of p-type cladding layer 16 and overgrowth 26, as shown in Figure 1C. P-type cladding layer 16 and the portion of the additional p-type cladding layer material grown on p-type cladding layer 16 collectively constitute p-type cladding layer 30. P-type cladding layer typically has a thickness about the same as that of n-type cladding layer 12, i.e., about 2 μm.

[0012] A p-contact layer (not shown) is grown on top of p-type cladding layer 30, and electrode layers (not shown) are deposited on the bottom surface of substrate 18 and the exposed surface of the p-contact layer. The electrode layers are then patterned to define electrodes. Layer structure 10 is then singulated into individual optoelectronic devices.

[0013] Although the above-described buried heterostructure waveguide provides performance advantages, the above-described fabrication process is complex and is difficult to control. In particular, it is essential to etch the layer structure using a

low-damage etch process, since the etch proceeds through the p-i-n junction formed by layers of p-type, undoped and n-type material (not shown) in active region 14. It is highly undesirable to have carrier states associated with structural defects in the etched sidewalls of the mesa. Moreover, the width of active region 14, i.e., the dimension of the active region in the x-direction shown in Figure 1A, is defined by the etch process. The width of the active region has to be accurately defined: too narrow an active region results in insufficient gain or too high a threshold current. Too wide an active region allows the optoelectronic device to operate in multiple optical modes, which is undesirable in many applications. Finally, the undercut profile of mesa 24 relative to mask 22 must also be accurately controlled to ensure that overgrowth 26 provides a reasonably planar surface on which to grow the additional p-type cladding layer material 28.

[0014] Optoelectronic devices for use in long wavelength telecommunications applications originally had indium gallium arsenide phosphide (InGaAsP) as the material of the quantum well layers. Using aluminum indium gallium arsenide (AlInGaAs) instead of InGaAsP as the material of the quantum well layers improves the high temperature characteristics of the optoelectronic device. However, using AlInGaAs as the material of the quantum well layers makes fabrication of the buried heterostructure waveguide structure considerably more difficult. This is because the presence of aluminum in the material of the quantum well layers leads to the formation of a stable layer of oxide on the sidewall of the mesa 24 during the wet etch. Unlike the less-stable oxides of indium and gallium formed when InGaAsP is etched, aluminum oxide cannot be thermally desorbed in the MOCVD growth chamber prior to growing overgrowth 26. Instead, the aluminum oxide layer persists on the sidewalls of the mesa, and degrades the quality of the interface between the mesa and overgrowth 26.

[0015] The problem of damage to the exposed sidewalls of the mesa 24 is exacerbated by the need to transfer the wafer from the etch station to the growth chamber after the etch process has been performed. The exposes the sidewalls of the mesa to ambient air, which typically contains water vapor and oxygen. The water vapor and oxygen can cause additional oxide formation on the sidewalls of the mesa.

[0016] Various approaches have been proposed to deal with the problem of stable

aluminum oxides forming on the sidewalls of the mesa. For example, in-situ etching may be used, as described by Bertone et al. in *Etching of InP-based MQW Structure in a MOCVD Reactor by Chlorinated Compounds*, 195 J. CRYST. GROWTH, 624 (1998). However, such approaches are expensive and difficult to implement, and may be incompatible with fabrication processes for other devices.

[0017] In *Densely Arrayed Eight-Wavelength Semiconductor Lasers Fabricated by Microarray Selective Epitaxy,* 5 IEEE J. SEL. TOP. QUANTUM ELECTRON., 428 (1999), K. Kudo et al. disclose a process for fabricating an array of buried heterostructure lasers using micro-selective area growth. This process is illustrated in Figures 2A-2C. Figure 2A shows a substrate 68 on which an n-type cladding layer 62 has been grown. An optical waveguide core mesa 80 that additionally constitutes the active region 64 of the optoelectronic device is then grown by micro-selective area growth on the surface of n-type cladding layer 62. The optical waveguide core mesa is grown in an elongate window 82 defined by two elongate mask patterns 84. The optical waveguide core mesa has a trapezoidal cross-sectional shape, and is elongate in the *y*-direction shown.

[0018] Using micro-selective area growth to fabricate an optical waveguide core mesa that includes the active region of a buried heterostructure laser improves the dimensional accuracy of the active region. Additionally, using micro-selective area growth forms the optical waveguide core mesa without the need to etch through the active region. However, a second micro-selective area growth process is used to cover optical waveguide core mesa 80 with p-type cladding material. The second micro-selective area growth process involves removing the wafer from the growth chamber and etching mask patterns 84 to increase the width of window 82. Figure 2B shows narrowed mask patterns 86 and widened window 88 resulting from etching the mask patterns 84 shown in Figure 2A.

[0019] The wafer is then returned to the growth chamber and a p-type cladding mesa 90 is grown over optical waveguide core mesa 80, as shown in Figure 2C. Cladding mesa 90 is grown by micro-selective area growth in the widened window 88 defined by narrowed mask patterns 86 on the surface of n-type cladding layer 62. Cladding mesa 90 has a trapezoidal cross-sectional shape and covers the sidewalls and top surface of optical waveguide core mesa 80.

[0020] Accordingly, although using micro-selective area growth to fabricate a buried heterostructure optoelectronic device obviates the need to etch through the active region itself, using a micro-selective area growth process that involves an intervening etch process, as disclosed by Kudo et al., does not provide a complete solution to the problems described above. The need to remove the wafer from the growth chamber to etch the mask patterns exposes the sidewalls of the optical waveguide core mesa to ambient air and, hence, to the possibility of stable oxide formation or other damage to the sidewalls. Additionally, the sidewalls of the optical waveguide core mesa are exposed to the etchant used to etch the mask patterns. This can result in stable oxide formation on, or other damage to, the sidewalls of the optical waveguide core mesa, especially when the quantum well structure contains aluminum. The devices disclosed by Kudo et al. had quantum well layers of InGaAsP.

[0021] Moreover, the optoelectronic devices fabricated by the process disclosed by Kudo et al. have a high inter-electrode capacitance because an appreciable area of cladding mesa 90 abuts n-type cladding layer 62. Finally, cladding mesa 90 has a relatively narrow top surface on which it is difficult to form the p-contact electrode.

[0022] Thus, what is needed is a way of fabricating optical waveguides and optoelectronic devices incorporating a buried heterostructure lateral waveguide structure that does not have the disadvantages of the buried heterostructure fabrication processes described above. What is also needed is a way of fabricating buried heterostructure optical waveguides and optoelectronic devices whose optical waveguide cores include aluminum. Finally, what is needed are optical waveguides and optoelectronic devices incorporating a buried heterostructure lateral waveguide structure that does not have the disadvantages of the buried heterostructure lateral waveguide structures described above.

Summary

[0023] The invention provides in a first aspect an optical waveguide or optoelectronic device that comprises a growth surface, a growth mask, an optical waveguide core mesa and a cladding layer. The growth mask is located on the growth surface and defines an elongate growth window. The optical waveguide core

mesa is located in the growth window and has a trapezoidal cross-sectional shape. The cladding layer covers the optical waveguide core mesa and extends over at least part of the growth mask.

[0024] The invention provides in a second aspect a device fabrication method in which a growth chamber is provided, a wafer having a growth surface is provided and a fabrication process is performed in the growth chamber. The fabrication process comprises growing an optical waveguide core mesa on the growth surface by micro-selective area growth, and, without removing the wafer from the growth chamber after fabricating the optical waveguide core mesa, covering the optical waveguide core mesa with cladding material.

[0025] The cladding material is grown without removing the substrate from the growth chamber by growing the cladding material under growth conditions in which the cladding layer material grows on the sidewalls of the optical waveguide core mesa in addition to the top surface of the mesa without the need to perform an etch process prior to growing the cladding material. The cladding material covering the optical waveguide core mesa protects the sidewalls of the optical waveguide core mesa from etchants and atmospheric contamination when the device is eventually removed from the growth chamber for further processing.

[0026] The invention provides in a third aspect a device fabrication method in which a wafer having a growth surface is provided, an optical waveguide core mesa is grown on the growth surface by micro-selective area growth at a first growth temperature and the optical waveguide core mesa is covered with cladding material at a second growth temperature, lower than the first growth temperature.

[0027] Covering the optical waveguide core mesa with the cladding material at the lower growth temperature allows the cladding material to grow on the sidewalls of the optical waveguide core mesa without the need to perform an etch process prior to growing the cladding material.

Brief Description of the Drawings

[0028] Figures 1A-1C illustrate the fabrication of a first type of prior art optoelectronic device incorporating a buried heterostructure optical waveguide.

Figures 2A-2C illustrate the fabrication of a second type of prior art

optoelectronic device incorporating a buried heterostructure optical waveguide.

Figures 3A-3G illustrate the fabrication of an optoelectronic device incorporating a buried heterostructure optical waveguide in accordance with an embodiment of the invention.

Figure 3H is an enlarged view of part of Figure 3F showing one sidewall of the optical waveguide core mesa.

Figure 4A is an isometric view of an exemplary embodiment of an optoelectronic device incorporating a buried heterostructure optical waveguide in accordance with the invention.

Figure 4B is an enlarged view of showing the structure of the optical waveguide core mesa of the exemplary optoelectronic device shown in Figure 4A.

Figures 5A and 5B are graphs showing some performance characteristics of an embodiment of an optoelectronic device in accordance with the invention configured as a buried heterostructure laser.

Detailed Description

[0029] The invention is based on the realization that the problems arising from exposing an optical waveguide core mesa grown by micro-selective area growth to an etchant and/or the atmosphere can be avoided by not widening the mask window before growing the p-type cladding layer. Instead, in accordance with the invention, the p-type cladding layer is grown under growth conditions that cause the p-type cladding layer material to grow on the sidewalls of the optical waveguide core mesa in addition to the top surface thereof. In accordance with an embodiment of the invention, after a thin layer of p-type cladding layer material has been grown on the top surface of the optical waveguide core mesa, the growth temperature is reduced to one at which the surface migration length of the p-type cladding material is less than the width of the sidewalls of the mesa. Under these growth conditions, the p-type cladding layer material grows not only on the top surface of the optical waveguide core mesa, but also on the sidewalls. This way, a p-type cladding layer that covers the sidewalls of the optical waveguide core mesa is grown before the wafer is exposed to an etchant and/or to the atmosphere or is subject to conditions that could otherwise damage the sidewalls of the optical waveguide core mesa.

[0030] Figures 3A-3G illustrate an exemplary embodiment of a method in accordance with the invention for making a device. In the example shown, an optoelectronic device is fabricated. Hundreds or thousands of optoelectronic devices are made at a time on a single wafer. The wafer is then singulated to yield the individual optoelectronic devices. Other embodiments of the method fabricate transparent waveguide devices, such as buried heterostructure optical waveguides.

[0031] Figure 3A is a side view of the small portion of a wafer 110 (Figure 3D) that constitutes the substrate 112 of an exemplary one of the optoelectronic devices fabricated on the wafer. The crystalline orientation on the major surface 114 of wafer 110 is [100]. In an exemplary embodiment, the material of the wafer is n-type indium phosphide (InP).

[0032] Wafer 110 is mounted on the susceptor (not shown) of a metal-organic chemical vapor deposition (MOCVD) growth chamber (not shown) and an n-type cladding layer 120 of n-type indium phosphide is grown on major surface 114, as shown in Figure 3B. The n-type cladding layer is grown to a thickness of about 2 μm. The exposed major surface of n-type cladding layer 120 provides a growth surface 122 on which an optical waveguide core mesa is grown.

[0033] A mask layer (not shown) is then deposited on growth surface 122. In an embodiment, the material of the mask layer was silicon dioxide (SiO_2). Wafer 110 is then removed from the growth chamber, and is subject to photolithography and etching to pattern the mask layer to define a growth mask 130, as shown in Figure 3C.

[0034] Figure 3D is a plan view of wafer 110 showing growth masks 130 arrayed on the growth surface 122 of n-type cladding layer 120 (Figure 3C) grown on the wafer. Each growth mask is composed of a pair of mask stripes 132. Figure 3D is highly simplified in the sense that it shows only three growth masks. In a practical embodiment, each growth mask 130 is about 10-25 μm wide, and adjacent growth masks are separated by a distance in the range from about 100 μm to about 500 μm across the width of the wafer, so a typical wafer has hundreds of growth masks arrayed on its surface. A flat 116 indicates the orientation of the [0-1-1] normal to the crystalline plane of the wafer.

[0035] Mask stripes 132 are elongate and have their long sides aligned parallel to

the [011] crystalline direction of growth surface 122, which is aligned in the *y*-direction shown. Each pair of adjacent ones of mask stripes 132 constitutes a growth mask 130 that defines an elongate growth window 134 in which an elongate waveguide core mesa will be grown by micro-selective area growth. The width of the growth window, defined by the distance in the *x*-direction between the opposed edges of the pair of the mask stripes 132, is in the range from about 1 μm and about 3 μm, and is typically in the range from about 1.5 μm to about 2 μm. The actual width of growth window 134 depends on the specified width of the quantum well structure of the optoelectronic device being made, i.e., the specified dimension in the *x*-direction of the quantum well structure.

[0036] Wafer 110 is returned to the MOCVD growth chamber, and optical waveguide core mesa 140 is grown in growth window 134 using micro-selective area growth. In the example of the optoelectronic device shown, optical waveguide core mesa 140 is structured to provide the active region of the optoelectronic device, and is composed of, in order from growth surface 122, an n-type buffer layer, a hole blocking layer, a substrate-side separation layer, a quantum well structure, a remote-side separation layer and an electron blocking layer. The structure of the optical waveguide core mesa will be described in detail below with reference to Figure 4B. At least one quantum well, composed of a quantum well layer (also shown in Figure 4B) sandwiched between two barrier layers (also shown in Figure 4B) is located in the quantum well region. In a transparent waveguide device, optical waveguide core mesa 140 is homogeneous and lacks the layers shown in Figure 4B.

[0037] During the growth of optical waveguide core mesa 140 by micro-selective area growth, semiconductor material formed from the precursors fed to the MOCVD growth chamber alights on growth mask 130. This semiconductor material does not nucleate on the growth mask, but migrates towards the portion of growth surface 122 exposed in growth window 134. The semiconductor material growing in the growth window has a strong tendency to form a [111] sidewall on which the growth rate is approximately zero. Accordingly, the semiconductor material grows predominantly on the top surface 146 of optical waveguide core mesa 140, and the optical waveguide core mesa grows in growth window 134 with the trapezoidal cross-sectional shape shown in Figure 3E. The optical waveguide core mesa is

bounded by straight, smooth, [111] sidewalls 144.

[0038] Growth of optical waveguide core mesa 140 is performed at a growth temperature at which the adatoms of the semiconductor material have sufficient mobility that their surface diffusion length is greater than the width *w* (Figure 3H) of the [111] surfaces constituting sidewalls 144. As long as the surface diffusion length is greater than the width of sidewalls 144, substantially no semiconductor material grows on the sidewalls.

[0039] Optical waveguide core mesa 140 is grown until it reaches its specified thickness. Then, the precursors fed to the growth chamber are changed to those for the p-type cladding layer material and the growth temperature is reduced slightly relative to that used to grow the optical waveguide core mesa. However, the reduced temperature is still above the temperature at which the surface diffusion length of the adatoms of the semiconductor material is greater than the width of sidewalls 144. Consequently, a thin sublayer 162 of the p-type cladding layer grows on the top surface of optical waveguide core mesa 140, as shown in Figure 3F.

[0040] After sublayer 162 of the p-type cladding layer has reached a thickness of a few tens of nanometers, the growth temperature is reduced to one at which the mobility of the adatoms of semiconductor material is such that their surface diffusion length is less than the width of sidewalls 144. Micro-selective area growth continues at the reduced growth temperature, and the semiconductor material continues not to nucleate on growth mask 130. However, at the reduced growth temperature, growth no longer predominantly occurs on the top surface 146 of optical waveguide core mesa 140. Consequently, the remainder of p-type cladding layer 160 grows on the sidewalls 144 of optical waveguide core mesa 140 in addition to growing on top surface 146.

[0041] Growth of p-type cladding layer 160 at the reduced growth temperature is continued until the p-type cladding layer reaches its specified thickness, as shown in Figure 3G. As the p-type cladding layer grows on sidewalls 144, it additionally extends laterally over part of growth mask 130. The p-type cladding layer forms a plane major surface 164 to which an electrode can later be applied.

[0042] After growth of p-type cladding layer 160 has been completed, wafer 110 is removed from the growth chamber. P-type cladding layer 160 covers the sidewalls

144 of optical waveguide core mesa 140 and therefore protects the sidewalls from the environment. Accordingly, the p-type cladding layer protects the sidewalls from damage during subsequent processing applied to the wafer, such as electrode application, electrode patterning and singulation.

[0043] Figure 4A is an isometric view of an exemplary embodiment of an optoelectronic device 100 in accordance with the invention fabricated by the above-described fabrication method in accordance with the invention. Figure 4A does not show the layer structure of the optical waveguide core mesa of optoelectronic device 100 to simplify the drawing. Figure 4B is an enlarged view of part of optoelectronic device 100 showing the layer structure of the optical waveguide core mesa.

[0044] Referring first to Figure 4A, optoelectronic device 100 is composed of a growth surface 122, a growth mask 130, an optical waveguide core mesa 140 and a cladding layer 160. Growth mask 130 is located on growth surface 122 and defines an elongate growth window 134. Optical waveguide core mesa 140 is located in the growth window and has a trapezoidal cross-sectional shape. Cladding layer 160 covers optical waveguide core 140 and at least part of growth mask 130.

[0045] In the example shown, growth surface 122 is the major surface of an n-type cladding layer 120 epitaxially grown on a substrate 112. In an embodiment, the material of substrate 112 is single-crystal n-type indium phosphide (InP), n-type cladding layer 120 is a layer of n-type InP and has a thickness of about 2 μm, and growth surface 122 has a [100] crystalline orientation.

[0046] In the example shown, growth mask 130 is composed of elongate, rectangular mask stripes 132. Mask stripes 132 are regions of silicon dioxide (SiO_2) having opposed parallel edges that define elongate growth window 134. Growth window 134 has a width in the range from about 1 μm to about 3 μm, and typically in the range from about 1.5 μm to about 2 μm . The actual width of the growth window is determined by the specified width of the quantum well region (154 in Figure 4B), the distance between growth surface 122 and the quantum well region, and the angle between sidewalls 144 and growth surface 122. Mask stripes 132 each have a width in the range from about 3 μm to about 11 μm. In the example shown, mask stripes 132 have a thickness of about 500 nm, which is similar (± 150 nm) to the height of optical waveguide core mesa 140. The opposed edges of the growth

stripes are aligned parallel to the [011] crystalline direction of growth surface 122.

[0047] An alternative material of growth mask 130 is silicon nitride Si_3N_4.

[0048] Optical waveguide core mesa 140 is located on the growth surface 122 of n-type cladding layer 120 in growth window 134 defined by growth mask 130. Optical waveguide core mesa is composed of one or more layers of one or more semiconductor materials having a higher refractive index than either of n-type cladding layer 120 and p-type cladding layer 160. In an embodiment, the refractive index contrast between optical waveguide core mesa 140 and cladding layers 120 and 160 was about -0.2. Optical waveguide core mesa 140 has a trapezoidal cross-sectional shape as a result of its fabrication by micro-selective area growth that forms [111] surfaces that constitute its sidewalls 144.

[0049] P-type cladding layer 160 covers optical waveguide core mesa 140 and at least part of growth mask 130. In particular, cladding layer 160 contacts sidewalls 144 of optical waveguide core mesa 140. In the example shown, the material of cladding layer 160 is p-type InP. Optical waveguide core mesa 140 is thus surrounded by n-type cladding layer 120 and p-type cladding layer 160, which have a greater refractive index than the materials of the optical waveguide core mesa. Thus, optical waveguide core mesa 140 and cladding layers 120 and 160 collectively constitute an optical waveguide.

[0050] In the example shown, optical waveguide core mesa 140 is structured to provide the active region of optoelectronic device 100. Figure 4B shows the structure of an example of such an optical waveguide core mesa140 composed of, in order, an n-type buffer layer 151, a hole blocking layer 152, a substrate-side separation layer 153, a quantum well structure 154, a remote-side separation layer 155 and an electron blocking layer 156. N-type buffer layer 151 is located on the growth surface 122 of n-type cladding layer 120. Blocking layers 152 and 156 are layers of semiconductor materials significantly higher in band gap energy than the semiconductor materials of separation layer 153 and 155. The structure composed of hole blocking layer 152, separation layers 153 and 155 and electron blocking layer 156 forms a separate confinement heterostructure (SCH) 159 that confines current carriers (i.e., electrons and holes) to quantum well structure 154.

[0051] N-type buffer layer 151 is a layer of n-type InP about 100 nm thick grown in

growth window 134 on growth surface 122 of n-type cladding layer 120.

[0052] Hole blocking layer 152 is a layer of n-type semiconductor material having a band gap energy higher than the materials of the adjacent layers, i.e., n-type buffer layer 151 and substrate-side separation layer 153. In an embodiment, hole blocking layer 152 was a layer of n-type aluminum indium arsenide (AlInAs) about 40 nm thick.

[0053] Substrate-side separation layer 153 is a layer of a semiconductor material having a band gap energy similar to that of the barrier layers of quantum well structure 154. No dopant was added to the material of the substrate-side separation layer during growth. In an embodiment, substrate-side separation layer 153 was a layer of AlGaInAs with Al, Ga and In fractions of 0.325, 0.175 and 0.5, respectively, about 50 nm thick.

[0054] Quantum well structure 154 is composed of N quantum well layers 157 interleaved with N+1 barrier layers 158, where N is a positive integer. In the example shown, N=7. The material of the quantum well layers has a substantially lower band gap energy that that of the barrier layers. No dopant is added to the materials of the quantum well structure during growth. In an embodiment, quantum well structure 154 was composed of seven quantum well layers 157, each about 9 nm thick, and eight barrier layers 158, each about 8 nm thick. The material of quantum well structure 154 was AlGaInAs with Al, Ga and In fractions of 0.18, 0.22 and 0.6, respectively, in quantum well layers 157 and 0.32, 0.22 and 0.46, respectively, in barrier layers 158.

[0055] Remote-side separation layer 155 is a layer of a semiconductor material having a band gap energy similar to that of barrier layers 158 of quantum well structure 154. No dopant is added to the material of the remote-side separation layer during growth. In an embodiment, remote-side separation layer 155 was a layer of AlGaInAs with Al, Ga and In fractions of 0.325, 0.175 and 0.5, respectively, about 50 nm thick.

[0056] Electron blocking layer 156 is a layer of p-type semiconductor material having a band gap energy higher than that of the materials of the adjacent layers, i.e., remote-side separation layer 155 and p-type cladding layer 160. In an embodiment, electron blocking layer 156 was a layer of p-type aluminum indium arsenide

(AlInAs) about 40 nm thick.

[0057] Referring again to Figure 4A, optoelectronic device 100 additionally has an electrode 172 located on the surface of substrate 112 remote from n-type cladding layer 120, an electrode 174 located on the surface 164 of p-type cladding layer 160, and opposed facets 176 and 178 disposed orthogonally to the long axis of optical waveguide core mesa 140. Facets 176 and 178 are typically formed by cleaving. In an embodiment of optoelectronic device 100 in which facets 176 and 178 are highly reflective, current flowing between electrodes 174 and 172 causes optoelectronic device 100 to operate as a laser and generate coherent light that is emitted through the facets. In an embodiment of optoelectronic device 100 in which facets 176 and 178 are coated with anti-reflective material, current flowing between electrode 174 and 172 causes optoelectronic device 100 to operate as an optical gain medium and generate light that is emitted through the facets. In another embodiment of optoelectronic device 100 in which facets 176 and 178 are coated with anti-reflective material, a voltage applied between electrode 172 and 174 causes optoelectronic device 100 to operate as an optoelectronic modulator with respect to light passing through the optical waveguide of which optical waveguide core mesa 140 forms part.

[0058] In optoelectronic device 100, n-type cladding layer 120, p-type cladding layer 160 and growth mask 130 form a capacitor that is a major contributor to the inter-electrode capacitance of optoelectronic device 100, i.e., the capacitance between electrodes 172 and 174. The growth mask constitutes the dielectric of the capacitor. Mask stripes 132 as thin as about 50 nm will reliably cover growth surface 122, and will therefore operate effectively as growth mask 130 in the micro-selective area growth process described above. However, using a thin growth mask can result in a high inter-electrode capacitance that limits the maximum modulation speed of the optoelectronic device. In the example of optoelectronic device 100 shown, growth mask 130 has a thickness greater than the minimum thickness required to cover growth surface 122 reliably. A thickness similar to that of optical waveguide core mesa 140, i.e., a thickness of about (500 ± ~150) nm , reduces the inter-electrode capacitance of optoelectronic device 100 to a level comparable with that of a conventional buried heterostructure optoelectronic device with a 3 μm-thick

InP:Fe cap layer. Such devices can be modulated at modulation speeds greater than 10 Gb/s.

[0059] Part of p-type cladding layer 160 abuts n-type buffer layer 151 and n-type hole blocking layer 152 (Figure 4B). However, this arrangement does not divert current away from quantum well structure 154 because the turn-on voltage the p-n junction between the p-type cladding layer and the n-type portions of optical waveguide mesa 140 type is greater than that of the p-i-n junction that includes the quantum well structure.

[0060] Fabrication of optoelectronic device 100 shown in Figure 4A will now be described in more detail with reference once again to Figures 3A-3H.

[0061] Referring first to Figure 3A, substrate 112 is part of a wafer 110 (Figure 3D) of n-type InP a few hundred micrometers thick. The material of the substrate is typically doped with sulfur (S). The crystalline orientation on the major surface 114 of the substrate is [100].

[0062] Whereas the material of substrate 112 is nominally the same as that of n-type cladding layer 120 (Figure 3B), its crystalline quality and purity is typically below that needed in the cladding layer of an optoelectronic device. Accordingly, wafer 110 is mounted on the susceptor in an MOCVD growth chamber and n-type cladding layer 120 is epitaxially grown on the major surface 114 of substrate 112 at a growth temperature of about 640 °C. N-type cladding layer is a layer of InP doped n-type with silicon. Typical precursors used to grow the n-type cladding layer are trimethylindium ($(CH_3)_3In$) and phosphine (PH_3) with disilane (Si_2H_6) as the silicon precursor. Growth continues until n-type cladding layer 120 reaches a thickness of about 2 μm. The surface of n-type cladding layer provides growth surface 122 whose crystalline orientation is [100].

[0063] If InP wafers with a crystalline quality and purity comparable with that of an epitaxially-grown layer are available, substrate 112 can serve as the n-type cladding layer of the optoelectronic device. In this case, no n-type cladding layer need be epitaxially grown on the substrate, and major surface 114 of the substrates provides the growth surface 122 on which optical waveguide core mesa 140 is grown by micro-selective area growth.

[0064] A mask layer (not shown as such) is then deposited on growth surface 122.

In the example shown, the mask layer is deposited on the surface of n-type cladding layer 120. In an embodiment, the material of the mask layer was silicon dioxide (SiO_2) formed using silane and oxygen as precursors. As noted above, the mask layer is typically deposited with a thickness of several hundred nanometers to reduce the inter-electrode capacitance of the optoelectronic device. This thickness is considerably thicker than the minimum thickness needed to reliably cover growth surface 122. In an embodiment, the mask layer had a thickness of 500 nm.

[0065] Wafer 110 is then removed from the growth chamber, and is subject to photolithography and etching to pattern the mask layer to define the mask stripes 132 shown in Figures 3C and 3D. Adjacent ones of the mask stripes collectively constitute a growth mask 130 that defines elongate growth window 134 on growth surface 122. Adjacent ones of the mask stripes 132 are separated by a distance, and, hence, growth window 134 has a width, in the range from about 1 μm and about 3 μm, and typically in the range from about 1.5 μm – 2 μm.

[0066] Mask stripes 132 have a width in the range from about 3 μm to about 11 μm, and typically in the range from about 5 μm to about 11 μm. Since semiconductor material that alights on growth mask 130 migrates towards the top surface 146 of optical waveguide core mesa 140 (Figure 3E) growing in growth window 134, mask stripes that are too wide result in a growth rate that is so fast that the thickness of the grown material is difficult to control. A high rate of growth is especially problematical towards the end of the process of growing the optical waveguide core mesa because the top surface 146 of the mesa is small in area. Consequently, so the growth rate is large and accelerating. On the other hand, mask stripes 132 that are too narrow allow the p-type cladding layers 160 grown on the optical waveguide core mesas in adjacent growth windows 134 to merge, which is also undesirable.

[0067] Once growth masks 130 have been formed, wafer 110 is returned to the growth chamber. The wafer is heated to a growth temperature of about 640 °C and optical waveguide core mesa 140 is grown by micro-selective area growth in growth window 134 defined on growth surface 122 by growth mask 130. Growth of an embodiment of optical waveguide core mesa 140 having the layer structure shown in Figure 4B will be described.

[0068] N-type buffer layer 151 is a layer of InP grown on growth surface 122. In the

example shown, growth surface 122 is the surface of n-type cladding layer 120. The n-type buffer layer is doped n-type with silicon. Typical precursors used to grow the n-type buffer layer are trimethylindium ($(CH_3)_3In$) and phosphine (PH_3) with disilane (Si_2H_6) as the silicon precursor. Growth continues until n-type buffer layer 151 reaches a thickness of about 100 nm.

[0069] N-type buffer layer 151 is made as thin as possible to reduce the total thickness of optical waveguide core mesa 140. Reducing the thickness of mesa 140 reduces the maximum growth rate of the mesa, i.e., the growth rate during deposition of sublayer 162 of p-type cladding layer 160 when the area of the top surface 146 of the mesa is a minimum. It is desirable to reduce the maximum growth rate to enhance control of the layer thickness and to maximize the crystalline quality of the material grown. Material that grows at a high growth rate can be of low crystalline quality because of strain.

[0070] In an embodiment in which the process of defining growth mask 130 in a layer of mask material does not degrade the crystalline quality of growth surface 122 and leaves no residue of the mask material in growth window 134, n-type buffer layer 151 need not be grown. In this case, hole blocking layer 152 is grown directly on growth surface 122. Omitting n-type buffer layer 151 desirably reduces the thickness of optical waveguide core mesa 140.

[0071] The supply of phosphine to the growth chamber is cut off, and supplies of trimethylaluminum ($(CH_3)_3Al$) and arsine (AsH_3) are commenced to grow hole blocking layer 152 of AlInAs on n-type buffer layer 151(or on growth surface 122, as noted above). The precursor flow rates are adjusted to produce the AlInAs with an aluminum fraction that provides lattice matching between the hole blocking layer and the InP of n-type buffer layer 151. Growth continues until hole blocking layer 152 reaches a thickness of about 40 nm.

[0072] A supply of trimethylgallium ($(CH_3)_3Ga$) is commenced to grow substrate-side separation layer 153 of AlGaInAs on hole blocking layer 152. The precursor flow rates are adjusted to produce the AlGaInAs with Al, Ga and In fractions of 0.325, 0.175 and 0.5, respectively. Material of this composition is lattice matched to InP. No dopant is added to the material of the substrate-side separation layer during growth. Growth continues until substrate-side separation layer 153 reaches a

thickness of about 50 nm.

[0073] Quantum well structure 154 is grown next. The precursor flow rates are first adjusted to grow a barrier layer 158 on substrate-side separation layer 153. Barrier layer 158 is a layer of AlGaInAs with Al, Ga and In fractions of 0.32, 0.22 and 0.46, respectively. Material of this composition has a band gap energy similar to that of the AlGaInAs of substrate-side separation layer 153 but has a different lattice constant so that the barrier layer is strained. No dopant is added to the material of the quantum well structure during growth. Growth continues until barrier layer 158 reaches a thickness of about 8 nm.

[0074] The precursor flow rates are then adjusted to grow a quantum well layer 157 on barrier layer 158. Quantum well layer 157 is a layer of AlGaInAs with Al, Ga and In fractions of 0.18, 0.22 and 0.6, respectively. Material with this composition has a band gap energy substantially lower than that of barrier layer 158. Such material also has a lattice constant that differs from that of the AlGaInAs of the substrate-side separation layer in the opposite direction from that of barrier layer 158 so that the quantum well layer is also strained. Growth continues until quantum well layer 157 reaches a thickness of about 9 nm.

[0075] The process, similar to that just described, of growing a barrier layer 158 followed by a quantum well layer 157 is repeated six times to grow a total of seven barrier layers and seven quantum well layers. The process, similar to that just described, of growing a barrier layer 158 is performed once to grow an eighth barrier layer. This completes growth of quantum well structure 154.

[0076] The precursor flow rates are then adjusted to grow remote-side separation layer 155 on quantum well structure 154. The precursor flow rates are adjusted to produce AlGaInAs with Al, Ga and In fractions of 0.325, 0.175 and 0.5, respectively. Material of this composition is lattice matched with InP, but is mis-matched with barrier layer 158. No dopant is added to the material of the remote-side separation layer during growth. Growth continues until remote-side separation layer 155 reaches a thickness of about 50 nm.

[0077] The supply of trimethylgallium to the growth chamber is cut off, and a supply of dimethylzinc ($(CH_3)_2Zn$) is commenced to grow electron blocking layer 156 of p-type AlInAs on remote-side separation layer 155, as shown in Figure 3E.

The precursor flow rates are adjusted to produce the AlInAs with an aluminum fraction that provides lattice matching to InP Growth continues until electron blocking layer 156 reaches a thickness of about 40 nm. This completes fabrication of optical waveguide core mesa 140.

[0078] The supplies of trimethylaluminum and arsine (AsH_3) to the growth chamber are cut off, a supply of phosphine (PH_3) is commenced, and the growth temperature is reduced to about 620 °C to grow sublayer 162 of p-type cladding layer 160, as shown in Figure 3F. Sublayer 162 is a thin layer of p-type InP and is grown on electron blocking layer 156 by micro-selective area growth. Sublayer 162 grows on the top surface 146 of optical waveguide core mesa 140.

[0079] The reduced growth temperature used to grow sublayer 162 of p-type cladding layer is still above the temperature at which the adatoms of the semiconductor material have sufficient mobility that their surface diffusion length is greater than the width *w* (Figure 3H) of the [111] surfaces constituting sidewalls 144. Thus, sublayer 162 grows predominantly on the top surface of optical waveguide core mesa 140 as just described. The growth temperature of about 620 °C can be used because the material being grown lacks aluminum. There is therefore is no need use a growth temperature of about 640 °C, which is needed when growing aluminum-containing materials to prevent aluminum from sticking to growth mask 130. The growth temperature of 620 °C is intermediate between the growth temperature used to grow optical waveguide core mesa 140 and the growth temperature used below to grow the remainder of p-type cladding layer 160. Growth of sublayer 162 continues until it reaches a thickness of a few tens of nanometers. In an embodiment, growth continued until sublayer 162 reached a thickness of about 40 nm.

[0080] The growth temperature is then reduced to about 600 °C. As the temperature falls, the adatoms of semiconductor material reduce in mobility so that their surface diffusion length becomes less than the width of the [111] surfaces constituting sidewalls 144. At the reduced growth temperature, micro-selective area growth continues but growth no longer occurs predominantly on the top surface 140 of optical waveguide core mesa 140. Instead, p-type cladding layer 160 additionally grows on the sidewalls 144 of the mesa. Growth of p-type cladding layer 160 at the

reduced growth temperature continues until the p-type cladding layer reaches its specified thickness, as shown in Figure 3G. In an embodiment, growth continued until p-type cladding layer 160 reached a thickness of 2 μm.

[0081] After the growth of p-type cladding layer 160 has been completed, wafer 110 is removed from the growth chamber. P-type cladding layer 160 covers the sidewalls 144 of optical waveguide core mesa 140 and extends over part of growth mask 130. Accordingly, the p-type cladding layer protects sidewalls 144 from damage during subsequent processing applied to the wafer. This processing includes deposition and patterning of electrodes 172 and 174, cleaving to form facets 176 and 178 and singulation into individual optoelectronic devices.

[0082] The invention is described above with reference to an example in which some of the semiconductor materials used to fabricate optical waveguide core mesa 140 comprise aluminum. However, this is not critical to the invention. None of the semiconductor materials used to fabricate the optical waveguide core mesa need comprise aluminum. For example, quantum well structure 154 may have quantum well layers 157 of InGaAsP. Lasers having such quantum well structures have a lower T_0 than those described above in which quantum well structure 154 has quantum well layers 157 of AlGaInAs.

[0083] The invention is described above with reference to examples in which optical waveguide core mesa 140 is structured to provide the active region of an optoelectronic device. However, embodiments of the invention is not limited to optoelectronic devices and their fabrication. The invention additionally encompasses transparent waveguide devices and their fabrication. Such embodiments of the invention provide transparent optical waveguides in which optical waveguide core mesa 140 has a trapezoidal cross-sectional shape but lacks the layer structure shown in Figure 4B. Instead, the optical waveguide core mesa is structured as a homogeneous mesa of a semiconductor material having a refractive index higher than that of cladding layers 120 and 160. Examples of suitable semiconductor materials include AlInAs, AlGaInAs and InGaAsP.

[0084] The invention is described above with reference to examples in which the opposed edges of growth mask 130 are described as being aligned parallel to the [011] crystalline direction of growth surface 122. However, although optimum

results are obtained with this alignment of the growth mask, micro-selective area growth is not critically dependent on alignment, and results that are acceptable for use in many applications are obtained notwithstanding a deviation from the parallel relationship described.

[0085] Figures 5A and 5B are graphs showing some performance characteristics of an embodiment of an optoelectronic device in accordance with the invention configured as a buried heterostructure laser. The laser generated light at a wavelength of 1350 nm and had a cavity length, i.e., distance between facets 176 and 178 (Figure 4A), of 300 μm. The material of the quantum well structure was AlGaInAs.

[0086] Figure 5A shows the variation of optical output power and forward voltage drop with current between electrodes 174 and 172 (Figure 4A) at ten different temperatures, 0 °C through 90 °C in ten-degree intervals. The laser had a threshold current of less than 4 mA at 0 °C and less than 20 mA at a temperature of 90 °C. The 0 °C threshold current is about 30% less than a conventional (Figure 1A-1C) InGaAsP BH laser.

[0087] Figure 5B shows the variation of c-w threshold current and differential quantum efficiency with temperature. The variation of both threshold current and efficiency with temperature is relatively small due to the higher characteristic temperatures obtained using AlGaInAs as the material of the quantum well structure. Sample lasers fabricated in accordance with the invention using AlGaInAs as the material of the quantum well structure had characteristic temperatures of T_0 (threshold current) = 55 °K and T_1 (efficiency) = 190 °K. An otherwise similar lasers fabricated in accordance with the invention using InGaAsP as the material of the quantum well structure had characteristic temperatures of T_0 = 45 °K and T_1 = 145 °K.

[0088] This disclosure describes the invention in detail using illustrative embodiments. However, the invention defined by the appended claims is not limited to the precise embodiments described.